

EV317136345

Inventor: Winston G. Scott  
Title: Methods of Forming Transistor Gates; and Methods of Forming Programmable Read-Only Memory Constructions  
Assignee: Micron Technology, Inc.

**INFORMATION DISCLOSURE STATEMENT**

**PURSUANT TO 37 C.F.R. §§1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation of co-pending application Serial No. 09/876,722 filed June 6, 2001. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 8/5/2003 Attorney: 

David G. Latwesen, Ph.D.  
Reg. #38,533  
WELLS ST. JOHN P.S.

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2375		PRIORITY SERIAL NO. 09/876,722		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Winston G. Scott				
				PRIORITY FILING DATE 6/6/01		PRIORITY GROUP 2812		
<b>U.S. PATENT DOCUMENTS</b>								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,033,952	03/00	Yasumura et al.				
	AB	6,124,168	9/2000	Ong				
	AC	5,668,705	11/97	Bergemont				
	AD	5,866,448	2/99	Pradeep et al.				
	AE	5,858,847	1/99	Zhou et al.				
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
<b>FOREIGN PATENT DOCUMENTS</b>								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
<b>OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AR		Watanabe, H. et al., "Novel $0.44\mu m^2$ Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application", IEEE 1998, pp. 36.2.1 - 36.2.4.					
	AS		Wolf, S., "Silicon Processing for the VLSI Era", Vol. 2, pp. 632-635.					
	AT		MITSUBISHI ELECTRIC WEBSITE: Reprinted from website <a href="http://www.mitsubisihelectric.com/r_and_d/tech_showcase/ls8.php">http://www.mitsubisihelectric.com/r_and_d/tech_showcase/ls8.php</a> on 3/29/2001: "8. Production Line Application of a Fine Hole Pattern-Formation Technology for Semiconductors", on 3/29/2001, 4 pgs.					
EXAMINER			DATE CONSIDERED					
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	AH							
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							Yes	No
	AM							
	AN							
	AO							
	AP							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from <a href="http://www.semiconductor.net/semiconductor/issues/1999/sep99/docs/feature1.asp">http://www.semiconductor.net/semiconductor/issues/1999/sep99/docs/feature1.asp</a> on 3/29/2001: "Resists Join the Sub-<math>\lambda</math> Revolution", 9 pgs.					
			1999/sep99/docs/feature1.asp on 3/29/2001: "Resists Join the Sub-<math>\lambda</math> Revolution", 9 pgs.					
	AS		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from <a href="http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp">http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp</a> on 3/29/2001: "Paths to Smaller Features", 1 pg.					
			1999/aug99/docs/lithography.asp on 3/29/2001: "Paths to Smaller Features", 1 pg.					
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